Claims 1-25 are pending in the subject application. Claims 1 and 20 have been amended to clarify the invention as claimed. The amendments are fully supported by the specification as originally filed.

Applicants claim a shift register for shifting an input pulse in synchronization with a clock signal, the clock signal being smaller in amplitude than a driving voltage of a control circuit, the shift register including: a plurality of flip flops, and a plurality of level shifters for level-shifting (i.e., increasing the voltage of) the clock signal, wherein at least one level shifter is provided for a predetermined number or block of flip flops.

Independent claims 1 and 20 both recite that when one of the flip flops (or a block of flip flop(s)) does not require input of the clock signal, the corresponding level shifter is suspended. The level shifter judges a period in which the clock signal must be received by its corresponding flip flop(s), and thus it is possible with the Applicants' invention to control operation of the level shifter based only on the start signal or the output of the previous step (see specification at page 21, second paragraph). According to this arrangement, a distance is reduced between the level shifter and flip flop, thereby simplifying the circuit design and reducing power consumption.

As shown in FIG. 1, the shift register 11 includes a plurality of flip flops $F1_{(1)}$... and corresponding level shifters $13_{(1)}$... which increase the voltage of a clock signal CK to the flip flops $F1_{(1)}$... When the flip flop $F1_{(i)}$ does not require input of a clock signal $CK_{(i)}$, operation of the level shifter $13_{(i)}$ is suspended. In such a state, the clock signal $CK_{(i)}$ is not driven, so that there is no power consumption required for driving.

Claims 1-25 were rejected under 35 USC 103(a) as being unpatentable over U.S. Patent 6,232,945 to Moriyama et al. (hereinafter "Moriyama") in view of U.S. Patent 6,081,131 to Ishii. This rejection is respectfully traversed.

Moriyama fails to teach or suggest a shift register having a plurality of level shifters for level-shifting a clock signal, where at least one level shifter is provided for a predetermined number or block of flip flops. As Moriyama fails to provide any disclosure of "a plurality of level shifters" as claimed, it also fails to teach or suggest wherein when one of the flip flops/blocks does not require input of the clock signal, the corresponding level shifter is suspended.

As shown in FIG. 17 of Moriyama, e.g., a display device and a shift register circuit 21 having a plurality of flip flops 22_1...22_{853} are connected in series, where each flip flop transfers a start pulse to its succeeding flip flop in synchronism with a clock pulse (see column 15, lines 11-19). There is no teaching or suggestion of providing a level shifter for each flip flop(s), as recited in the Applicants' claimed invention.

Ishii also fails to teach or suggest a plurality of level shifters, where one of the level shifters is provided for a corresponding number or block of flip flops. With reference to FIG. 8, Ishii teaches level shifters 51 and 53, and 52 and 54, respectively, which are provided outside the drivers 48 and 44, respectively. The level shifters 51 and 53, for example, are structured differently and function in a manner different from the Applicants' claimed invention. Level shifter 51 generates a horizontal start signal HST and transmits the signal to the driver 48; level shifter 53 generates horizontal clock signals HCK1 and HCK2 and transmits such signals to the driver 48 (see column 14, lines 51-65). Such level shifters are not associated with any flip flop and do not transmit an input pulse in synchronization with a clock signal. In fact, the horizontal start signal HST and the clock signals HCK1 and HCK2 must first reach the horizontal system driver 48 before they can be combined.

In contrast, the Applicants' claimed invention requires that at least one level shifter must be provided corresponding to each flip flop or block of flip flops. Further, there is no mechanism disclosed in Ishii for suspending one of the level shifters when a corresponding flip flop does not require input of the clock signal.

The combined teachings of Moriyama in view of Ishii fail to teach or suggest the Applicants' claimed invention, e.g., as recited in claims 1 and 20. There is no teaching or suggestion in Ishii for providing a level shifter that is connected to a corresponding predetermined number or block of flip flops, and thus one of ordinary skill in the art could not combine Moriyama and Ishii in such a manner.

For the above reasons, the claims should now be in condition for immediate allowance. However, if there are any outstanding issues, the Examiner is urged to call the undersigned at the phone number listed below.

The Applicants believe that additional fees are not required for consideration of the within Amendment. However, if for any reason a fee is required, a fee paid is inadequate or credit is owed for any excess fee paid, you are hereby authorized and requested to charge Deposit Account No. **04-1105**.

Respectfully submitted,
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APPENDIX A:
VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Claims 1 and 20 have been amended as follows:

1. (Amended) A shift register for shifting an input pulse in synchronization with a clock signal, the clock signal being smaller in amplitude than a driving voltage of a control circuit, comprising:

flip flops of a plurality of steps that output [a signal] the input pulse in synchronization with [a] the clock signal, said flip flops being divided into a plurality of blocks, each of the blocks including at least one of said flip flops; and

a plurality of level shifters, one of the level shifters corresponding to each of the blocks, the level shifters for increasing [a] the voltage of [a] the clock signal [smaller in an amplitude than a driving voltage of said flip flop] and for applying the clock signal to each of said flip flops, said shift register transmitting [an] the input pulse in synchronization with the clock signal,

[wherein said flip flops are divided into a plurality of blocks, each including at least one of said flip flops,

said level shifter is provided for each of said blocks, and

among a plurality of said level shifters, at least one of said level shifters, which correspond to blocks requiring no clock signal input for transmitting the input pulse,] wherein when one of the blocks does not require input of the clock signal, the corresponding level shifter is suspended at that point.

20. (Amended) A shift register, in which a plurality of flip flops are connected, for transmitting an input pulse in synchronization with a clock signal [and for outputting a signal], the clock signal being smaller in amplitude than a driving voltage of a control circuit, comprising:

[said shift register comprising] a plurality of level shifters for level-shifting the clock signal, [said] wherein at least one level shifter [being] is provided for [every] a

predetermined number of said flip flops, the level shifters for increasing the voltage of the clock signal and for applying the clock signal to each of the flip flops,

wherein when one of the flip flops does not require input of the clock signal, the corresponding level shifter is suspended at that point.